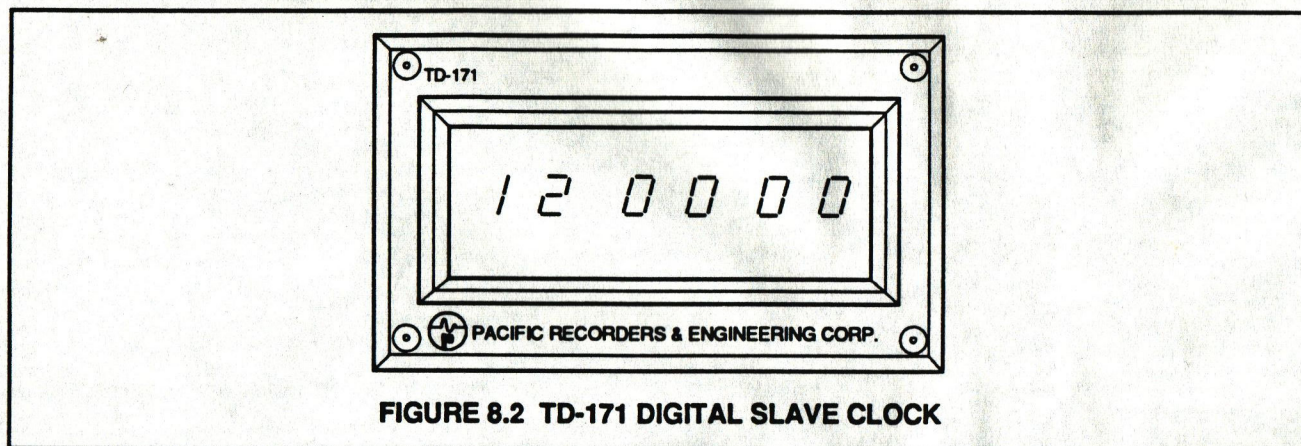


## 8.1.2 TD-171 Digital Slave Clock

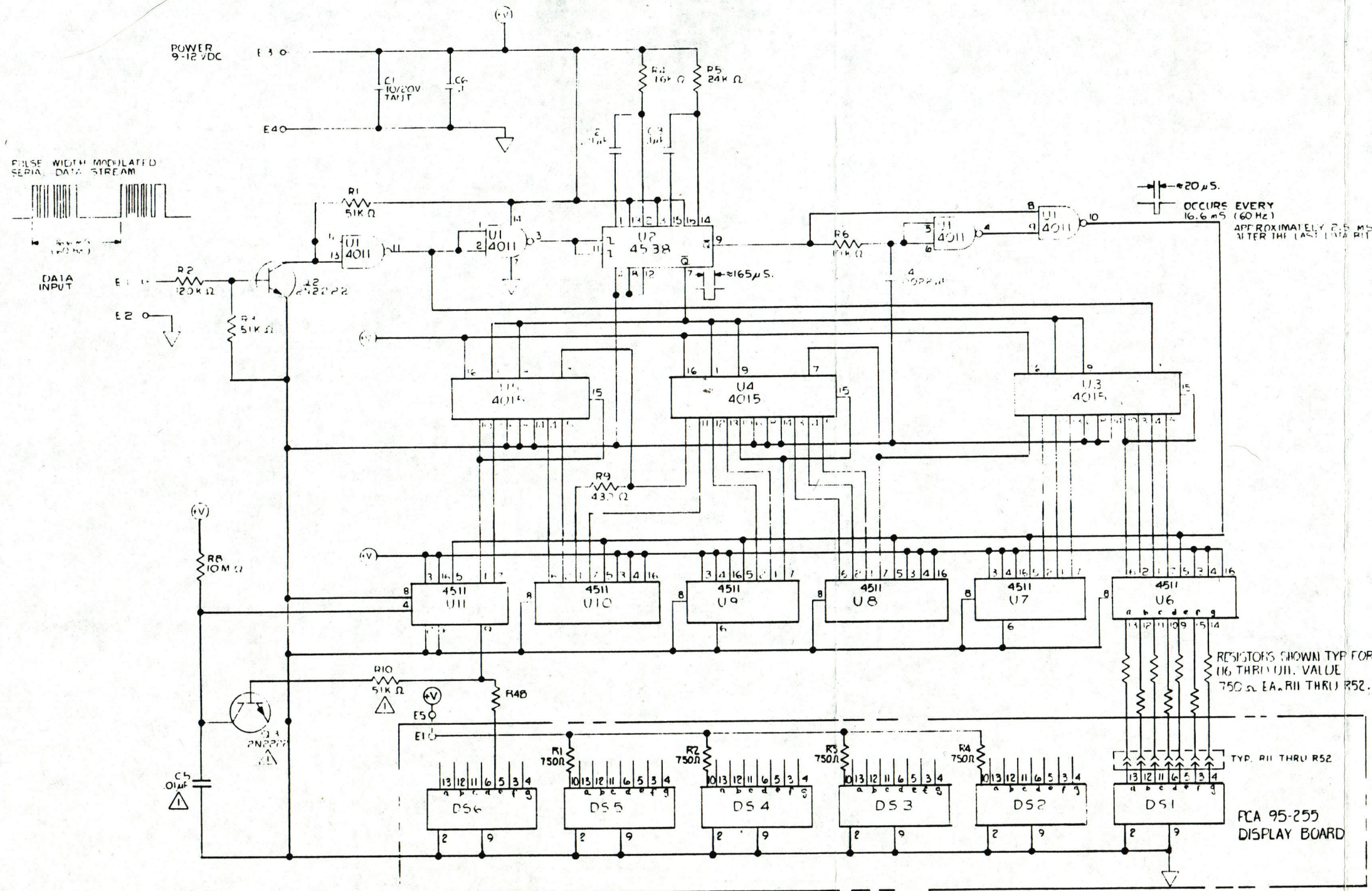
The TD-171 Digital Slave Clock is a six-digit (hours, minutes, seconds) digital display specifically designed to operate with an ESE or compatible master clock time code generator. It is constructed in an aluminum case for shielding, uses an external power supply (PR&E #50-17, supplied with the clock), and is designed specifically for use in PR&E consoles. Power and master clock connection are made to the rear of the unit.



### CIRCUITRY

The TD-171 circuit is virtually the same as the ESE model ES-171 unit (the TD-171 is manufactured with the express consent of ESE). The time code consists of 24 bits of pulse width modulated data. A wide pulse (260 microseconds) represents a binary one (1), and a narrow pulse (65 microseconds) represents a binary zero. The data rate is 60 Hz.

Demodulation is accomplished using shift registers U3, U4 and U5. The incoming data is buffered by transistor Q2 and gate U1 before it is fed to shift register U3. One of the one-shots of dual monostable U2 is used to clock the shift registers. The pulse width of this one-shot is set to be 2.5 times the pulse width of the narrow data pulse. As a result a "one" or "zero" will be clocked into U3 depending on the width of the data pulse. The second one-shot of U2 is retriggered by each data pulse until the completion of all 24 bits of data. U2 then times out and triggers another one-shot, formed by two gates of U1. This transfers the data from the shift register outputs to the latches contained in decoder/drivers U6 through U11, prior to the next transmission of data. This completes the serial-to-parallel conversion. The decoder/drivers and displays then translate the parallel BCD information into the visual time display.



20µS.  
OCCURS EVERY 16.6ms  
APPROXIMATELY 2.5 MSP  
AFTER THE LAST DATA BIT

