OPERATING & MAINTENANCE INSTRUCTION MANUAL

MODEL 215

BROADCAST AUDIO PROCESSOR

INOVONICS
INCORPORATED

USER'S RECORD

Model 215-___-___-___, S/N ______

Date Purchased ________________

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INSTRUCTION MANUAL

MODEL 215

MULTIFUNCTION AUDIO PROCESSOR

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I. GENERAL INFORMATION

The Inovonics 215 is a broadband audio processor primarily intended for AM, FM and TV broadcast use, although certain features make it attractive also for sound re-enforcement and some studio recording situations.

The 215 presents an as-needed approach to audio processing, as the basic unit consists of a chassis supplied with signal bypass assemblies. Plug-in options then provide the three processing functions of (1) gated, gain-riding A.G.C., (2) average level compression and (3) peak control with phase-optimization and asymmetrical operation for AM broadcast, or variable frequency-selective characteristics for FM broadcast and recording.

Options may be provided singly to perform specific processing functions or to complement existing equipment, or the 215 may be "fully-loaded" and stand alone as a complete processing system.

II. FUNCTIONAL DESCRIPTION AND SPECIFICATIONS

A description of each of the three processing functions of the 215 follows. Specifications relative to the described subsection are given in the text. Performance data not expressed or implied in the descriptions is tabulated at the end of this section.

Gated A.G.C. (-01 option)

In the typical broadcast situation, program levels tend to wander up and down a bit, frequently as a result of operator inattention, personnel shift changes or from other, usually human influences. Thus the first major functional block of the 215 is a slow, gain-riding A.G.C. This effectively erases long-term input level variations and presents subsequent processing stages with a constant r.m.s. input value.

Capture range of the A.G.C. is ±10dB, and A.G.C. gain may be selectively displayed on the front panel meter. Correction rate (response time) is about 0.5dB/second, slow enough not to alter program dynamics.

A frequency-weighted "gating" feature inhibits A.G.C. action during program pauses, and slowly returns gain to 0dB in event of extended signal loss. The gating circuit has -3dB sensitivity points at 300Hz and 3kHz to guard against erroneous gain "hunting" caused by non-program noises. Gating threshold sensitivity is preset at a value which will open the gate when midband program energy rises above -25dB relative to nominal program "zero" level.

It is generally acknowledged that program components below a particular frequency contribute nothing to perceived program quality and, in fact, may sabotage intelligibility and both perceived and measured program loudness. The choice of a low-end cutoff frequency is, nevertheless, a matter for subjective consideration; thus the 215 offers three: 50, 70 and 100Hz. The L.F. cutoff frequency is selected with a series of straps on the A.G.C. Amplifier board. Strapping instructions are given on page 9.

A digitally-generated, pseudo-random Pink Noise generator is an integral part of the 215 A.G.C. Amplifier assembly. Pink Noise is a very useful audio test signal; its constant-power-per-octave (or equal fractions thereof) energy distribution and characteristic crest factor more closely approximate program material than do discrete oscillator tones. A switch substitutes this test signal for the input program in any operating mode to aid in system setup and maintenance.

Average Level Compressor (-02 option)

Program dynamics are firmly-yet-unobtrusively compressed by the 215's averaging Compressor assembly. This circuit utilizes gain-control circuitry yielding a "soft knee," or gentle transition from linear to compressed operation. In fact, the actual compression ratio increases as more compression is employed. With 10dB or so of indicated compression the ratio is about 2:1, increasing to 4:1 at 15dB. The result of this program-controlled compression ratio is an exceedingly smooth sound, even with considerable compression in effect. Nevertheless, a control loop from the Compressor back to the A.G.C. circuit guards against overcompression by reducing A.G.C. gain and flashing a warning indicator when the Compressor works too hard. Compressor attack and release times are fixed at values insuring an optimum, rapid operation consistent with an acceptable distortion figure at low frequencies.

The AM "Integrated" Peak Controller (-03 option)

Asymmetrical modulation of positive and negative peaks yields a modulation advantage only when the program material is asymmetrical in nature. Most music, because it is a blend of complex waveforms which are not phase-related, has a very even balance of peak energies. Solo instruments and the human voice, on the other hand, possess a more or less fixed relationship between the phase of the fundamental tone and the harmonics. This leads to an appreciable and consistent imbalance between positive and negative peaks, and can be used to modulation advantage.

To maintain optimum asymmetrical modulation of an AM carrier, program peaks should be predominantly positive-going. Current practice is to switch program phase whenever necessary to assure the highest incidence of positive modulation. Common phase-switching techniques usually cause an annoying "click" or "pop" at the instant of reversal. The Phase-Follower of the 215, on the other hand, features a novel "phase-rotation" circuit which gently and inaudibly "rolls" the phase through a 180-degree shift when required for maximum positive modulation. Sensitivity of the phase-detection circuit of the Phase-Follower is fixed, yet a function of the degree of peak limiting/clipping in effect. With a consistent 10dB of peak reduction, asymmetry of 10% will cause a phase reversal. With 15dB peak reduction, 5% asymmetry will initiate a "roll."

The 215 AM Peak Controller represents the most radical departure from previous processor peak reduction systems. To satisfy the particular requirements for optimum AM carrier modulation, an interrelated peak limiter/clipper circuit functions without compromising the features of either. Here is the basic principle of its operation: the output from the Phase-Follower is fed to a true, low-distortion peak limiter of the Santana configuration. This is followed by an active hard clipper with the unique ability to quantitatively monitor the degree of clipping it performs. This information is routed back to the peak limiter through a control loop which allows adjustment of the limiting/clipping ratio. "Clipping Depth" may be set to a desired value, and once set will remain constant regardless of program content. An optimum operating peak-to-average ratio may thus be selected, from a very clean signal without audible clipping, to a slight degree of clipping for a definite gain in loudness with negligible sacrifice in listenability, or even heavier clipping for decided modulation advantage with an attendant audible harshness, particularly on voice.

Because of the interrelated limiter/clipper circuit, Peak Controller attack time is virtually instantaneous. Even the first half-cycle of a 20kHz, 20dB overload is reduced to the final limited peak value. The release time is fixed at a value which yields less than 1% distortion at 50Hz with 10dB limiting. Nevertheless, a strap on the Peak Controller board permits a speed-up in release time by a factor of 4. The result is a tradeoff: an audible modulation advantage against an increase in low frequency distortion. The 1% distortion frequency moves up to 200Hz, and distortion at 50Hz increases to about 3%. Both Peak Limiting and Clipping Depth may be selectively displayed on the front panel meter.

The 215 permits the value of positive modulation peaks to be continuously adjusted up to 150% of the negative peak value. Although positive modulation is legally restricted to 125%, many plate-modulated transmitters require drive in excess of +125% to reach the legal maximum. It must be warned, however, that transmitters which fall into this category are incapable of linear operation up to +125%. The very slight gain in perceived signal loudness must be weighed against probable high signal distortion in these cases.

An active Low-Pass Filter follows the AM Peak Controller and serves to restrict the bandwidth of the processor output. Higher-order harmonics generated in the limiting/clipping process are significantly attenuated, thus substantially reducing the tendency for the modulated carrier to "splatter" into adjacent frequencies. Moreover, transmitter power is not wasted in modulating those audio frequencies normally lost in the AM broadcast receiver. An H.F. cutoff frequency of 7, 10 or 15kHz may be selected. Selection is made with a series of straps on the circuit board; instructions are given on page 9.

<u>The FM Peak Controller</u> (-04 option)

The FM Peak Controller is very similar to the AM assembly in the concept of an "integrated" limiter/clipper, but the phase-following, asymmetrical modulation features are, of course, not included. Instead, complementary pre-limiting pre-emphasis and post-limiting de-emphasis are employed to satisfy the requirements of FM broadcast pre-emphasis. A series of circuit board straps permit selection of the standard 75µs, "Dolby" 25µs or "flat" characteristics.

The optional, faster release time selection and variable Clipping Depth features are retained in the FM Peak Controller, but it is anticipated that these will be used conservatively (if at all) in FM broadcasting. The low-pass filter which follows the limiting circuitry is fixed for a high-end roll-off beginning just above 15kHz.

"Proof" Mode

A single button places the 215 in "Proof." The A.G.C. is defeated and Compressor inhibited. The Peak Controller is similarly defeated, and both the High- and Low-Pass Filters are electronically set to their obvious extremes. All signal-path circuitry is otherwise active.

Stereo Interconnection

Two 215's may be interconnected for stereo operation. Compressors are slaved for identical operation, and one Phase Follower may be slaved to the other or both defeated, depending on which system of AM-stereo transmission is ultimately approved.

215 Specifications

This is a tabulation of those performance specifications which are not expressed in the texts of the foregoing discussions.

Frequency Response: ±1dB, 50Hz-15kHz

Distortion (with 10dB Compression and 10dB Limiting-only): <0.3% THD above 200Hz, <1.0% THD at 50Hz.

Noise: Better than 60dB below 100% modulation.

Input: Balanced, -30 to +10dBm

Output: Balanced, 0 to +20dBm; +24dBm output clipping level.

Power: 105-130VAC (230V available), 50/60Hz, 20W

Physical: 3-1/2" x 19" x 9"; 8 lbs.

III. INSTALLATION

Unpacking and Inspection

Upon receipt of the equipment, inspect at once for shipping damage. Should any such damage be observed, notify the carrier at once; if not, proceed as outlined below. It is suggested that the original shipping carton and materials be retained should future reshipment become necessary. In the event of return for Warranty repair, shipping damage sustained as a result of improper packing for return may invalidate the Warranty.

It is important that the Warranty Registration card found at the front of this manual be returned; for not only does this assure coverage of the equipment under terms of the Warranty, but the user will automatically receive specific servicing or modification information should it be issued.

Mounting

The 215 is packaged to mount in a standard 19-inch equipment rack, requiring 3-1/2 inches of rack space per unit. The processor generates negligible heat, and itself is unaffected by wide variations in the ambient operating temperature.

RFI

The 215 is specifically designed to operate in close proximity to broadcast transmitters; nevertheless, care should be exercised in locating the unit away from abnormally high RF fields. In some installation situations an RF ground loop may be formed between the input or output cable shield grounds and the AC power cord ground. Use of a "ground-lifting" AC adapter should remedy the problem, but the chassis of the unit should somehow be returned to earth ground for safety.

In/Out Connection and Considerations

The 215 input and output connections are brought out to a rear panel screw-terminal barrier strip. Both the input and output are balanced (transformer-isolated), with ground terminals provided for cable shields.

Should the equipment which feeds the 215 require output loading, an external 600-ohm resistor should be placed across the processor's input terminals; otherwise the input is "balanced-bridging" with a characteristic input impedance of 10K or more.

The source impedance of the 215 output amplifier (ahead of the line output transformer) is virtually zero. However, as the output transformer has some reactance, it is important that the output be terminated in 600 ohms to minimize overshoot.

The output clipping level of the 215 is +24dBm. To permit positive peak excursions to reach +125%, the nominal 100%-modulation sine wave output level should be kept at +18dBm or below.

Polarity

The input and output of the 215 are each marked with + and - designations to aid in maintaining proper phase in stereo applications, or proper asymmetrical modulation of program peaks. In the latter case, the + output terminal will be positive-going with positive modulation peaks.

IV. OPERATION AND ADJUSTMENT

The various adjustments are identified on the inside of the removable front adjustment cover. Despite the seemingly obvious meanings of the control function descriptions, it is highly recommended that the outlined procedure be carefully followed for initial setup. Subsequent readjustment to secure a desired effect should be made only after it has been established that the unit functions properly and predictably in accordance with the initial setup procedure.

All adjustments are made "on the air," utilizing a typical program feed and the station Modulation Monitor.

Preliminary - P.C.B. Strapping Options

Input Gain Range

The 215 accommodates line input levels between -30 and +10dBm. To extend resolution of the INPUT GAIN control, the overall 40dB range is broken into two, 20dB ranges selected by a strap on the A.G.C. Amplifier P.C.B., or Peak Controller P.C.B. if the A.G.C. and Compressor options are not used.

For line input levels between -30 and -10dBm, a strap should be placed across terminals A and B. For input levels between -10 and +10dBm, the strap should be removed.

High-Pass Filter

Strapping to select the 215 low-end rolloff frequency is afforded on the A.G.C. Amplifier P.C.B. The three cutoff frequencies are 50, 70 and 100Hz.

For 50Hz cutoff, no strap is required. For 70Hz, strap C to D. For 100Hz cutoff, strap C to D to E. The H.P.F. is automatically defeated in the "Proof" mode.

Low-Pass Filter

Strapping to select the high-end rolloff frequency is afforded on the AM Peak Controller P.C.B. only. The three cutoff frequencies are 7, 10 and 15kHz.

For 15kHz rolloff, strap E to F to H and, separately, J to K to L. For 10kHz rolloff, strap E to F and, separately, J to K. For 7kHz rolloff, no strap is required. The L.P.F. is automatically defeated in the "Proof" mode.

Peak Limiter Release

The limiter portion of the Peak Controller has a release time selected and fixed at a value which is an optimum compromise between high perceived loudness (fast release) and low signal distortion (slow release). With 10dB limiting, the compromise release value yields about 1% distortion of a 50Hz sine wave; correspondingly less distortion at higher frequencies.

An alternate, faster limiter release time is provided; its optional use can result in a perceptible increase in program loudness, but at the expense of greater low frequency signal distortion. Because the selectable high-pass filter is provided on the A.G.C. amplifier, however, a user can opt to roll the low frequencies off and utilize the faster release with no apparent program degradation.

The faster release time is enabled by strapping terminals M and N on the AM Peak Controller P.C.B., and F and H on the FM version. As previously cautioned, this should be done in conjunction with 70 or 100Hz low-end rolloff.

Suggested Initial Setup Procedure

This procedure is performed with the 215 in the program chain, "on the air" and fed with typical program material. For convenience, this procedure also appears inside the front cover of the unit.

1. Turn all trim controls fully counterclockwise. The PROOF and PINK NOISE buttons should be "out" (normal position).

2. Depress the A.G.C. RANGE metering button. With a normal program input, advance the INPUT GAIN control for a center-scale meter indication.

3. Adjust the COMPRESSION slide pot for an indicated

compression of about 10dB.

4. Depress the PEAK LIMITING metering button. Advance the PEAK DRIVE control for an indicated 5-10dB of peak reduction.

5. Advance the OUTPUT LEVEL control for negative modulation peaks of 95-100% as indicated by the Modulation Monitor.

6. Advance the POSITIVE PEAK AMPLITUDE control for desired positive peak modulation to 125% as indicated by the Modulation Monitor.

Clipping Depth

The degree of program clipping which the user wished to employ in is made variable with the CLIP DEPTH control. This adjustment is made subjectively, and the final setting should be arrived at only after sampling all types of program material.

By depressing the CLIPPING DEPTH metering button, a more-or-less quantative indication of clipping depth is displayed on the front panel meter. With the pointer remaining in the "white" zone, clipping is very light and inaudible with any program material. When the pointer indicates in the "gray" area, clipping is heavier and yields a definite modulation advantage. Some "harshness" may be audible on voice, however. When the meter indicates in the "black", clipping is quite heavy and will certainly be audible, probably objectionable on voice and even some music.

V. CIRCUIT DESCRIPTIONS

A.G.C. Amplifier

Input signals to the 215 are isolated by input transformer T2 on the "mother" board, then fed to input amplifier IC2 on the A.G.C. Amplifier assembly. The 40dB input gain range is divided into two 20dB segments by strapping R1 in or out, and the INPUT GAIN control R4 gives 20dB variable control over the input signal.

TEST switch S1 selects between the normal program input and the internal Pink Noise test signal generator. IC1 is a monolithic, pseudo-random, digital "white" noise source. The filter comprised of R6-9 and C2-5 imparts a 3dB/octave falling characteristic to the noise, yielding "Pink Noise" with constant-power-per-octave bandwidth.

The second section of IC2 is the active, selectable high-pass filter. The 50, 70 or 100Hz rolloff frequency is selected by strapping terminal D, or both D and E to terminal C, essentially at ground via FET Q8. Q8 is turned off in the "Proof" mode to return the filter to 50Hz, "full bandwidth" response.

The first half of IC3 is the active gain control element of the A.G.C. Amplifier. This circuit, the "Santana" configuration, utilizes FET Q1A as an active variable resistance across the inverting input of the operational amplifier. Q1B, a parameter-matched "dummy" FET, is placed across the non-inverting amplifier input and cancels the channel non-linearities of Q1A. This permits control of the audio signal at levels which would otherwise be above the low distortion operating range of the FETs.

Q4 and 5 comprise a "Baxandall" full-wave rectifier. The positive-going portion of the output of variable-gain stage IC3 is amplified by common-emitter stage Q4, the negative-going by common-base stage Q5. Thus equal positive and negative information cause similar currents at the collector junction. Q6 imparts additional DC gain to the rectified signal which is then filtered by the network R31/C16 and R32/C17. The long time constant of this dual filter prevents the A.G.C. circuit from following the program envelope, insuring control over only long-term signal variations. IC5, a unity-gain buffer amplifier, isolates the filter from R33, the FET pinchoff calibration adjustment.

Output from the A.G.C. variable-gain stage is sampled by the Gating Circuit. The first half of IC4 is a bandwidth-limited voltage amplifier stage with -3dB points at 300Hz and 3kHz. This insures that the amplified signal will primarily consist of legitimate program material, rather than non-program noise. This signal is rectified by CR5 and 6, the resultant DC presented to one input of a comparator utilizing the second half of IC4. The other comparator input is held at a fixed DC potential by divider R41/42 with a small amount of positive feedback through R43 to impart hysteresis to the Gating function.

Gating logic is fed back to the Baxandall rectifier circuit to return the A.G.C. amplifier to a nominal 0dB gain figure when the program signal falls below the Gating threshold. The circuit is thus prevented from slowly raising residual noise to an annoying level during program pauses.

IC6 is a comparator which constantly monitors the Compressor "overcomp" bus. Should the Compressor average more than about 15dB compression, IC6 will toggle to illuminate the OVERCOMP indicator and to override A.G.C. action and reduce circuit gain. The A.G.C. amplifier and Gating circuits are inhibited in the "Proof" mode via CR10 and 11.

The second half of IC3 and transistors Q2 and 3 form an output stage to feed the Compressor assembly. Terminals H and F, must be strapped when this assembly is used in the 215; the RC network thus shorted is required for use with the Model 231 Multiband Audio Processor.

Average Level Compressor

An input signal of constant long-term level from the A.G.C. Amplifier assembly is routed to the Compressor assembly via R3, the COMPRESSION control. R3 affords ±12dB control over the input to the Compressor, and a corresponding control over the amount of compression in effect. The first half of IC1 buffers the input signal and drives the variable-gain stage.

Q5, with its current-source collector load Q6, is, in effect, a single-stage operational amplifier. Gain of this stage is roughly set by the value ratio between input resistor R13 and feedback resistor R15. Amplifier gain is varied by Q4, the saturation resistance shunting the amplifier summing mode to ground.

Transistor saturation resistance is not symmetrical, if a transistor were placed in the ground leg of a typical resistance voltage divider, an AC signal would be severely distorted. The single stage operational amplifier, on the other hand, is simultaneously depleted of loop gain as the input signal is shunted, assuming a non-linear characteristic cancelling that of the saturation transistor. Gain reduction is thus effected without distortion.

The output from the compressor is buffered by half of IC2 and fed to a "precision" full-wave rectifier composed of IC3 and associated components. Q3, normally on, is turned off in the "Proof" mode to inhibit compression.

The rectified signal is buffered by Q9 and filtered by C10 and R44. The time constant is selected for optimum response vs. distortion. Half of IC2 further buffers the filtered DC to drive both the gain-controlling transistor Q4 and the front-panel meter through its linearizing network of CR13 and 14, R48 and 49.

The second half of IC1 buffers the compressed program signal and feeds the Peak Controller.

AM Peak Controller

The Compressor output feeds the summing mode of the Peak Controller input amplifier IC1. The one half of IC1 is a voltage amplifier stage for signals from the Compressor assembly. Variable feedback resistor R4 is the LIMITER DRIVE control and affords a 20dB drive adjustment.

The other half of IC1 provides additional voltage gain for the Phase Follower detector and control circuit. Positive and negative peaks are rectified by CR1 and 2, respectively, and held by associated capacitors C5 and 6. R17 and 18 sum the peak levels such that the polarity of DC across C7 will represent program peak predominance. One half of IC5 monitors this DC and toggles (with a certain fixed hysteresis) to provide polarity switching logic.

FET-input IC2 performs the phase "rotation" function. With the non-inverting input held at ground through FET Q1, IC2 inverts the program signal. When Q1 is off, the program polarity is not inverted. Q1 is turned on and off slowly through the RC network of R28 and C8 to provide an inaudible 180-degree program phase reversal. IC3 buffers the signal appearing across Q1 to "linearize" the FET DC control voltage for minimum signal distortion during the actual period of phase "rotation." The remaining half of IC5 drives the front-panel POLARITY indicators.

Q2 and one half of IC4 comprise a "Santana" configuration, the linear gain-control portion of the Peak Controller. The Santana circuit is described on page 12. The output of this circuit is fed to the bases of transistors Q6 and 7. The emitters of these devices are biased a few volts positive and negative, respectively, and the base-emitter junctions provide hard clipping of the program signal. The emitter bias of Q7 can be varied to provide asymmetrical peak clipping for increased positive modulation.

In addition to their clipping duties, Q6 and 7 further perform a rectification function to control gain of the Santana Circuit. Q8, a unity-gain inverter, follows Q7 to provide the same polarity of collector current for negative-going peaks as Q6 does for positive. Q9 gives additional control loop gain which is made variable with CLIPPING DEPTH control R57. Thus a signal composed of (and proportional to) the clipped portion of the program signal is rectified, filtered by R63, 64 and C14, buffered by one half of IC4 and used to vary program gain prior to clipping. In this way the degree of program clipping can be kept constant regardless of program content. When R57 is fully CCW (minimum resistance) control loop gain is at maximum so that virtually no measurable clipping at all results in linear gain reduction. Increasing the value of R57 reduces control loop gain so that Q6 and 7 must conduct harder to effect gain reduction; this increases clipping action.

Output from the limiter/clipper is routed to the variable low-pass filter. This consists of one half of IC6, C9 and 10 and the various resistors which can be strapped for high-end cutoff frequencies of 7kHz (no straps), 10kHz (E to F and J to K), or 15kHz (E to F to H and J to K to L.)

The remaining half of IC6, along with Q4 and 5 and associated circuitry, makes up the line output amplifier. Gain is variable over a 20dB range with OUTPUT LEVEL control R38. Chassis-mounted output transformer T3 permits "balanced" operation.

FM Peak Controller

The Compressor output feeds the summing mode of the Peak Controller input amplifier IC1. The one half of IC1 is a voltage amplifier stage for signals from the Compressor assembly. Variable feedback resistor R4 is the LIMITER DRIVE control and affords a 20dB drive adjustment.

The second half of IC1 provides pre-limiting pre-emphasis. Proper strapping of terminals C, D and E selects either a 25 or 75µs characteristic.

Q1 and one half of IC2 comprise a "Santana" configuration, the linear gain-control portion of the Peak Controller. The Santana circuit is described on page 12. The output of this circuit is fed to the bases of transistors Q5 and 6. The emitters of these devices are biased a few volts positive and negative, respectively, and the base-emitter junctions provide hard clipping of the program signal. In addition to their clipping duties, however, Q5 and 6 further perform a rectification function to control gain of the Santana circuit. Q7, a unity-gain inverter, follows Q6 to provide the same polarity of collector current for negative-going peaks as Q5 does for positive. Q8 gives additional control loop gain which is made variable with CLIPPING DEPTH control R34. Thus a signal composed of (and proportional to) the clipped portion of the program signal is rectified, filtered by R40, 41 and C13, buffered by one half of IC2 and used to vary program gain prior to clipping. In this way the degree of program clipping can be kept constant regardless of program content. When R34 is fully CCW (minimum resistance), control loop gain is at maximum so that virtually no measurable clipping at all results in linear gain reduction. Increasing the value of R34 reduces control loop gain so that Q5 and 6 must conduct harder to affect gain reduction; this increases clipping action.

Output from the limiter/clipper is routed to the low-pass filter comprised of R15 and 16, C6 and 7 and one half of IC3. This filter begins its high-end rolloff just above 15kHz. The remaining half of IC3, along with Q3 and 4 and associated circuitry makes up the line output amplifier. Gain is variable over a 20dB range with OUTPUT LEVEL control R17. Capacitors C8 and 9 can be selectively strapped across feedback resistor R40 to provide 25 or 75µs de-emphasis, complementary to the pre-limiting pre-emphasis.

Bypass Assemblies

Two plug-in "bypass" cards may be used in place of the various functional assemblies in the 215, so that any one assembly or pair of assemblies may be used alone. One card has no active circuitry, and merely routes the input-to-output. This card is used to bypass the A.G.C. Amplifier assembly, the Compressor assembly or both assemblies.

The other bypass card includes an input amplifier and an output line-drive amplifier, and is used to replace the Peak Controller assembly only. The first half of IC1 accepts input signals directly at its summing mode from a preceeding Compressor assembly or via an input resistor network if the Compressor has been bypassed. In the latter case, terminals A and B can be strapped if necessary to increase input gain by 20dB. OUTPUT control R4 provides 20dB of variable gain.

Terminals C and D, associated with the output amplifier, afford a 10dB gain change. Between the A to B, C to D strappings and the variable control, the Peak Controller bypass assembly can be assigned any value of circuit gain which may be required in an installation situation.

Power Supply

The 215 Power Supply consists of chassis-mounted power transformer T1 and rectifier and regulator components mounted on the Power Supply PC board.

Diodes CR1-4 and filter capacitors C1 and 2 provide the raw positive and negative DC supplies. Total supply regulation is the function of two "three-terminal" monolithic regulators, IC1 and 2.

The Power Supply assembly also includes the pushbutton switches for power, "Proof" mode and metering selection.

VI. CALLIBRATION PROCEDURES

NOTE: Prior to shipment from the factory, the 215 was "burned-in" for an appropriate period and carefully aligned utilizing calibrated test gear and special fixtures to facilitate adjustment. As the processor contains no components suseptable to ageing, routine alignment is discouraged. Field calibration should be restricted to those instances in which a circuit failure has necessitated replacement of critical components.

EQUIPMENT REQUIRED

1. Stable Audio Oscillator, H.P. 200 CD or equivalent.
2. AC Voltmeter with dB scale, H.P. 400 D or equiv.
3. Oscilloscope with lmHz bandwidth.
4. Processor Extender Card

A.G.C. Amplifier Assembly

A. Preliminary

1. Connect the oscillator to the 215 input.
2. Extend the A.G.C. Amplifier assembly.
3. Make a temporary connection to the "top" of R24. This is the A.G.C. assembly output and should be connected to the AC voltmeter. Be sure the other side of the voltmeter input is returned to ground.
4. Connect clip leads or other temporary shorts across R27, R32 and R47.

B. FET Null and Pinchoff

1. Turn R33 fully CW.
2. Apply lkHz at a level which yields 0dBm output.
3. Turn R33 fully CCW and adjust R18 for a null. The

null should reach at least -60dBm.

4. Turn R33 fully CW. The reading should return to about 0dBm. Turn R55 CCW for a 0.25dB decrease in the actual voltmeter indication.

5. Remove the shorts from R27 and R47 only.

C. Meter Cal.

1. Disconnect the oscillator. The GATE lamp should go out.

2. Depress the A.G.C. RANGE button. When the meter reaches equilibrium, adjust R34 for a center-scale (center of grey area) indication.

D. Pink Noise Cal.

1. Remove the short from across R32.

2. Depress the PINK NOISE button and adjust R12 for a center-scale indication on the A.G.C. meter. Circuit action will be slow, so wait for the indication to stabilize during adjustment.

E. R21 Adjustment

R21 is adjusted after the Compressor assembly has been calibrated. With the COMPRESSION slide pot centered, R21 is adjusted for 10dB indicated compression with the Pink Noise test signal. R21 can otherwise be left in the center of its rotation.

Compressor Assembly

A. Preliminary

1. Remove the A.G.C. Amplifier assembly from the processor during calibration of the Compressor assembly.

2. Attach a temporary connection to the end of R4 farthest from the adjusting screw on the Peak Controller Assemblies, or nearest the screw on the Bypass card. This is the output of the combining amplifier and should be fed to the AC voltmeter. Be sure the other side of the voltmeter input is returned to ground. R4 (PEAK

DRIVE) on the Peak Controller assembly should be fully CW during this Compressor calibration.

3. The oscillator is fed to the top terminal of the COMPRESSION slide pot R3. Be sure the other side of the oscillator is returned to ground.

B. Output Level Adjustment

1. Center slide pot R3, place the 215 in "Proof."

2. Set the oscillator frequency to 1kHz, oscillator output level to -10dBm

3. Adjust R32 for a reading of 0dBm from the combining amplifier.

4. Remove the 215 from the "Proof" mode.

C. Compression Ratio Cal. and Meter Cal.

1. With slide pot R3 centered and -10dBm at 1kHz from the oscillator, adjust R45 for a reading of -10dBm at the output of the combining amplifier.

2. Adjust R47 for a front panel COMPRESSION meter indication of 10dB.

3. After the Compressor assembly has been calibrated and the A.G.C. Amplifier card installed, R21 on the A.G.C. Amplifier card can be adjusted as described on page 19 for 10dB indicated compression.

AM Peak Controller

A. Preliminary

1. Remove the Compressor assembly from the 215.

2. Extend the Peak Controller assembly and make temporary connection to terminal A. There should be no jumper between terminals A and B. Terminal A serves as the signal imput for calibration purposes and should be connected to the oscillator output. Be sure the other side of the oscillator

output is returned to ground.

3. Connect the AC voltmeter to the 215 output.

B. FET Null and Pinchoff

1. Place the 215 in "Proof." Turn both the LIMIT DRIVE control R4 and the OUTPUT LEVEL control R38 fully CCW.

2. Apply 1kHz to the terminal A input point at a level of -8dBm.

3. Turn R65 fully CW. The monitored output should measure 0dBm ±1dB. Reset the oscillator output for a reading of exactly 0dBm.

4. Turn R65 fully CCW and adjust R9 for a null. The null should reach at least -40dBm.

5. Turn R65 fully CW. The reading should return to 0dBm. Turn R65 CCW for a 0.25dB decrease in the actual voltmeter indication.

C. Meter Calibration

1. Depress the PEAK LIMITING meter selector button and adjust R67 for a full-scale "zero" indication.

2. Depress the CLIPPING DEPTH button and adjust R60 for a full-scale "zero" indication.

3. Remove the 215 from the "Proof" mode.

D. Rectifier Balance

1. Turn both the POS. PEAK AMPL. control R53 and the CLIP DEPTH control R57 fully CCW.

2. Depress the PEAK LIMITING button and advance the 1kHz oscillator amplitude for an indicated 10dB of limiting.

3. Connect the 'scope probe to the "top" of R61. A baseline of about -6V with a positive-going pulse train should be observed.

4. Rotate R52 through its range. At one point near the center of rotation the pulse repetition rate

should double. Set R52 at this "doubling" point and for equal successive peaks.

FM Peak Controller

A. Preliminary

1. Remove the Compressor assembly from the 215.

2. Extend the Peak Controller assembly and make temporary connection to terminal A. There should be no jumper between terminals A and B. Terminal A serves as the signal input for calibration purposes and should be connected to the oscillator output. Be sure the other side of the oscillator output is returned to ground.

3. Connect the AC voltmeter to the 215 output.

B. FET Null and Pinchoff

1. Place the 215 in "Proof." Turn both the LIMIT DRIVE control R4 and the OUTPUT LEVEL control R17 fully CCW.

2. Apply 1kHz to the terminal A input point at a level of -8dBm.

3. Turn R42 fully CW. The monitored output should measure 0dBm, ±1dB. Reset the oscillator output for a reading of exactly 0dBm.

4. Turn R42 fully CCW and adjust R8 for a null. The null should reach at lease -40dBm.

5. Turn R42 fully CW. The reading should return to 0dBm. Turn R42 CCW for a 0.25dB decrease in the actual voltmeter indication.

C. Meter Calibration

1. Depress the PEAK LIMITING meter selector button and adjust R44 for a full-scale "zero" indication.

2. Depress the CLIPPING DEPTH button and adjust R37 for a full-scale "zero" indication.

3. Remove the 215 from the "Proof" mode.

D. Rectifier Balance

1. Turn the CLIP DEPTH control R34 fully CCW.

2. Depress the PEAK LIMITING button and advance the 1kHz oscillator amplitude for an indicated 10dB of limiting.

3. Connect the 'scope probe to the "top" of R38. A baseline of about -6V with a positive-going pulse train should be observed.

4. Rotate R29 through its range. At one point near the center of rotation the pulse repetition rate should double. Set R29 at this "doubling" point and for equal successive peaks.

VII. APPENDIX

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
		A.G.C. BOARD (A/N 147700)		
C1,17	1070	Capacitor, Tantalum 47uF, 20V	Matsuo	221L-2002-476M7
C2	0863	" Mylar .022uF, 100V	Sprague	225P22391
C3,8,9	0867	" Mylar .1uF, 100V	"	225P10491
C4,10,14,15	1065	" Tantalum .22uF, 35V	Matsuo	DTSA-3502-224M
C5	1067	" Tantalum 1uF, 35V	"	DTSA-3502-105M
C6,18,19	1053	" Tantalum 2.2uF, 20V	"	DTSA-2002-225M
C7	0801	" Mica 10pF	Arco	DM15-100J
C11	0816	" Mica 330pF	Arco	DM15-331J
C12	0858	" Mylar .0047uF, 100V	Sprague	225P47291
C13,16	1054	" Tantalum 4.7uF, 20V	Matsuo	DTSA-2002-475M
CR 1-13	1100	Diode, Silicon	G.E.	1N4151
IC1	1351	Integrated Circuit, Type MM5837	National	
IC2-4,6	1313/ 1314	" " Type RC4558NB/ NE5535N	Raytheon/ Signetics	
IC5	1352	" " Type LF355N	National	
J1-5	1685	IC Sockets, 8 pin DIP	Augat	308-AG37-D
Q1A,1B,8	1211	Transistor, FET MPF111	Siliconix	
Q2,4,5	1204	" 2N3567	Fairchild	
Q3,6,7	1205	" 2N3645	Fairchild	

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
R4	0514	Resistor, Variable 100K	Beckman	89PR100K
R12	0564	" " 200K	"	91AR200K
R18	0554	" " 200 ohm	"	91AR200
R21	0556	" " 1K	"	91AR1K
R33,34	0559	" " 10K	"	91AR10K
		All fixed resistors are 1/4W carbon, value and tolerance per schematic.		
S1	1841	Switch, Single Pushbutton	Schadow	FG EE FG/Wht
		COMPRESSOR ASSEMBLY (A/N 147500)		
C3,5,6,10	1054	Capacitor, Tantalum 4.7uF, 20V	Matsuo	DTSA-2002-475M
C4	1069	" Tantalum 220uF, 6.3V	Matsuo	22IL-6301-227M7
C9,11,12	1053	" Tantalum 2.2uF, 20V	Matsuo	DTSA-2002-225M
CR3,6-14	1100	Diode, Silicon, Signal	G.E.	1N4151
IC 1-3	1313	Integrated Circuit, Type 4558	Raytheon	
J 1-3	1685	IC Socket, 8 pin DIP	Augat	308-AG37-D
Q3	1211	Transistor, MPF111	Siliconix	
Q4,6,9	1205	" 2N3645	Fairchild	
Q5	1210	" SE4010	Fairchild	

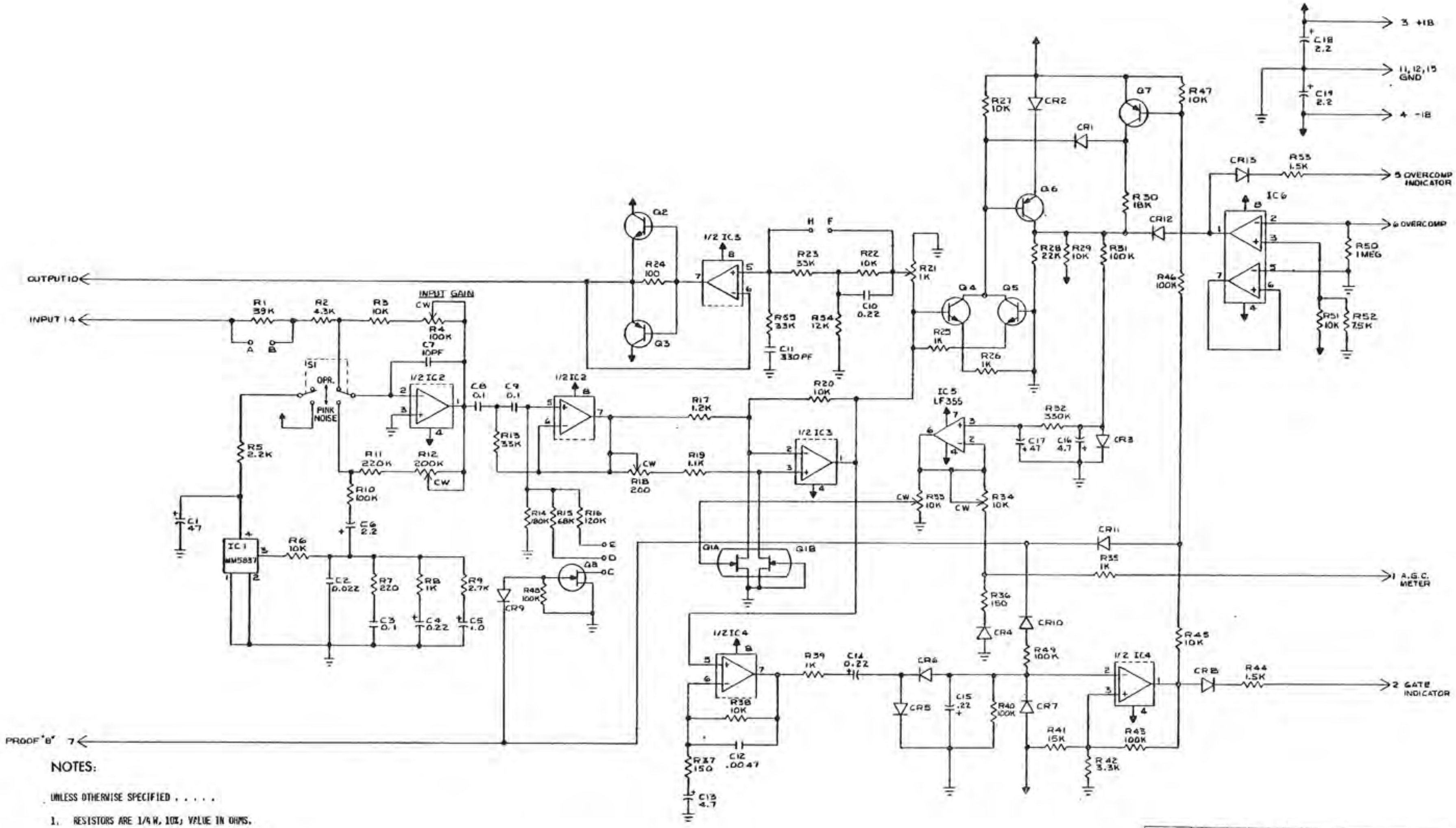
SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
R3	0616	Resistor, Variable, "Slide" 10K	CTS	LM2842
R32,45	0563	" " Trim 100K	Beckman	91AR100K
R47	0559	" " " 10K	Beckman	91AR10K
		All fixed resistors are 1/4W carbon, value and tolerance per schematic.		
		AM PEAK CONTROLLER ASSEMBLY (A/N 147000)		
C1	0801	Capacitor, Mica 10pF	Arco	DM15-100J
C2	0850	" Mylar .001uF, 100V	Sprague	225P10291
C3,4	1070	" Tantalum 47uF, 20V	Matsuo	22IL-2002-476M7
C5,6,15,16	1053	" Tantalum 2.2uF, 20V	Matsuo	DTSA-2002-225M
C7	0867	" Mylar .1uF, 100V	Sprague	225P10491
C8,13	1054	" Tantalum 4.7uF, 20V	Matsuo	DTSA-2002-475M
C9	0827	" Mica 300pF	Arco	DM15-301J
C10	0812	" Mica 150pF	Arco	DM15-151J
C11,12	1069	" Tantalum 220uF, 6.3V	Matsuo	221L-6301-227M7
C14	1067	" Tantalum 1uF, 35V	Matsuo	DTSA-3502-105M
CR 1-13	1100	Diode, Silicon	G.E.	1N4151
IC1,4-6	1313/ 1314	Integrated Circuit, Type RC4558NB/ NE5535N	Raytheon Signetics	
IC2,3	1352	" " Type LF355N	National	

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
J1-4	1685	IC Sockets, 8 pin DIP	Augat	308-AG37-D
Q1,2A,2B,3	1211	Transistor, FET MPF111	Siliconix	
Q4,6,8,11	1204	" 2N3567	Fairchild	
Q5,7,9,10	1205	" 2N3645	Fairchild	
R4,38	0514	Resistor, Variable 100K	Beckman	89PR100K
R9,52	0554	" " 200 ohm	"	91AR200
R53	0506	" " 500 ohm	"	89PR500
R57	0510	" " 10K	"	89PR10K
R60,65,67	0559	" " 10K	"	91AR10K
		All fixed resistors are 1/4W carbon, value and tolerance per schematic.		
		<u>FM PEAK CONTROLLER ASSEMBLY</u> (A/N 150900)		
C1	0801	Capacitor, Mica 10pF	Arco	DM15-100J
C2	0858	" Mylar .0047uF, 100V	Sprague	225P47291
C3	0854	" Mylar .0022uF, 100V	Sprague	225P22291
C4,5	1070	" Tantalum 47uF, 20V	Matsuo	221L-2002-476M7
C6	0827	" Mica 300pF	Arco	DM15-301J
C7	0812	" Mica 150pF	Arco	DM15-151J
C8	0834/ 0855	" Mylar 2700pF/ .0027uF, 100V	Arco/ Sprague	DM19-272J/ 225P27291
C9	0851/ 0823	" Mylar .0012, 100V/ 1200pF	Sprague/ Arco	225P12291/ DM19-122J

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
C10,11	1069	Capacitor, Tantalum 220uF, 6.3V	Matsuo	22IL-6301-227M7
C12	1054	" Tantalum 4.7uF, 20V	Matsuo	DTSA-2002-475M
C13	1067	" Tantalum 1uF, 35V	Matsuo	DTSA-3502-105M
C14,15	1053	" Tantalum 2.2uF, 20V	Matsuo	DTSA-2002-225M
CR1-9	1100	Diode, Silicon Signal	G.E.	1N4151
IC1-3	1313/ 1314	Integrated Circuit, Type RC4558NB/ NE5535N	Raytheon Signetics	
Q1A,B	1211	Transistor, FET (matched pair) MPF111	Siliconix	
Q2	1211	" " MPF111	"	
Q3,5,7	1204	" NPN, 2N3567	Fairchild	
Q4,6,8,9	1205	" PNP, 2N3645	"	
Q10	1210	" NPN, SE4010	"	
R4,17	0514	Resistor, Multiturn Variable 100K	Beckman	89PR100K
R8,29	0554	" Variable Trimmer 200 ohm	"	91AR200
R34	0510	" Multiturn Variable 10K	"	89PR10K
R37,42,44	0559	" Variable Trimmer 10K	"	91AR10K
		All fixed resistors are 1/4W carbon, value and tolerance per schematic.		

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
		PEAK BYPASS ASSEMBLY (A/N 152000A)		
C1	0801	Capacitor, Mica 10pF	Arco	DM15-100J
C2	1070	" Tantalum 47uF, 20V	Matsuo	221L-2002-476M7
C3,4	1053	" Tantalum 2.2uF, 20V	Matsuo	DTSA-2002-225M
CR1-4	1100	Diode, Silicon	G.E.	1N4151
IC1	1313	Integrated Circuit, Type RC4558NB	Raytheon	
Q1	1204	Transistor, 2N3567	Fairchild	
Q2	1205	" 2N3645	Fairchild	
R4	0514	Resistor, Variable 100K	Beckman	89PR100K
		All fixed resistors are 1/4W carbon, value and tolerance per schematic.		
		POWER SUPPLY BOARD (A/N 147300), LED BOARD (A/N 147900), MOTHER BOARD (A/N 151200) and CHASSIS ASSY.		
C1,2	0910	Capacitor, Electrolytic 500uF, 50V	Sprague	TVA 1315
C3,4	1053	" Tantalum 2.2uF, 20V	Matsuo	DTSA-2002-225M
C5-10	1064	" Ceramic 0.005uF, 1kV	Sprague	5GA-D50
CR1-4	1125	Diode, Silicon	Motorola	1N4005
CR5	1100	" "	G.E.	1N4151

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
I1,2	2015	LED Indicator, Green	Litronix	GL 4850
I3,4	2014	" " Red	"	RL 4850
IC1	1311	Integrated Circuit, Type 7818	National	LM7818C
IC2	1312	" " Type 7918	Signetics	UA7918C
J1 (P.S./LED) J6,7 (M.B.)	1686	IC Socket, 16 pin DIP	Augat	316-AG37D
J1,2,3 (M.B.)	1708	PC Socket, 15 pin Single-edge	SAE	SAC-15S/2-2
J4 (P.S.)	1692	Connector, 2 pin Male	Molex	09-88-2021
J5 (M.B.)	1781	Barrier Strip, 6 Terminal	Cinch	6-140-Y
M1	2806	Meter, Edgewise "Compression"		
M2	2807	Meter, "Limiting - Clipping - A.G.C."		
	--	All fixed resistors are 1/4W carbon, value and tolerance per schematic.		
S1	1840	Switch, Multi-station Pushbutton	Schadow	5FA15FA201/ BLK-GRN 2UGR
T1	148200	Transformer, Power	Triad	F90-X
T2	1502	" Input	Microtran	MT11-A
	1503	Shield for T2	"	M90
T3	109000	Transformer, Output		



NOTES:

UNLESS OTHERWISE SPECIFIED . . . . .

1. RESISTORS ARE 1/4 W, 10%; VALUE IN OHMS.
2. CAPACITORS ARE 20 V, OR BETTER, VALUE IN µF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV.).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF111 ").
6. DIODES ARE P/N 1100 (1N4005 EQUIV.)
7. IC'S ARE P/N 1315 (TYPE 5535/4558

215 231	DRAWN	FAK	1-25-79
	CHECKED		
	APPROVED		
TOLERANCES	MATERIAL / FINISH		

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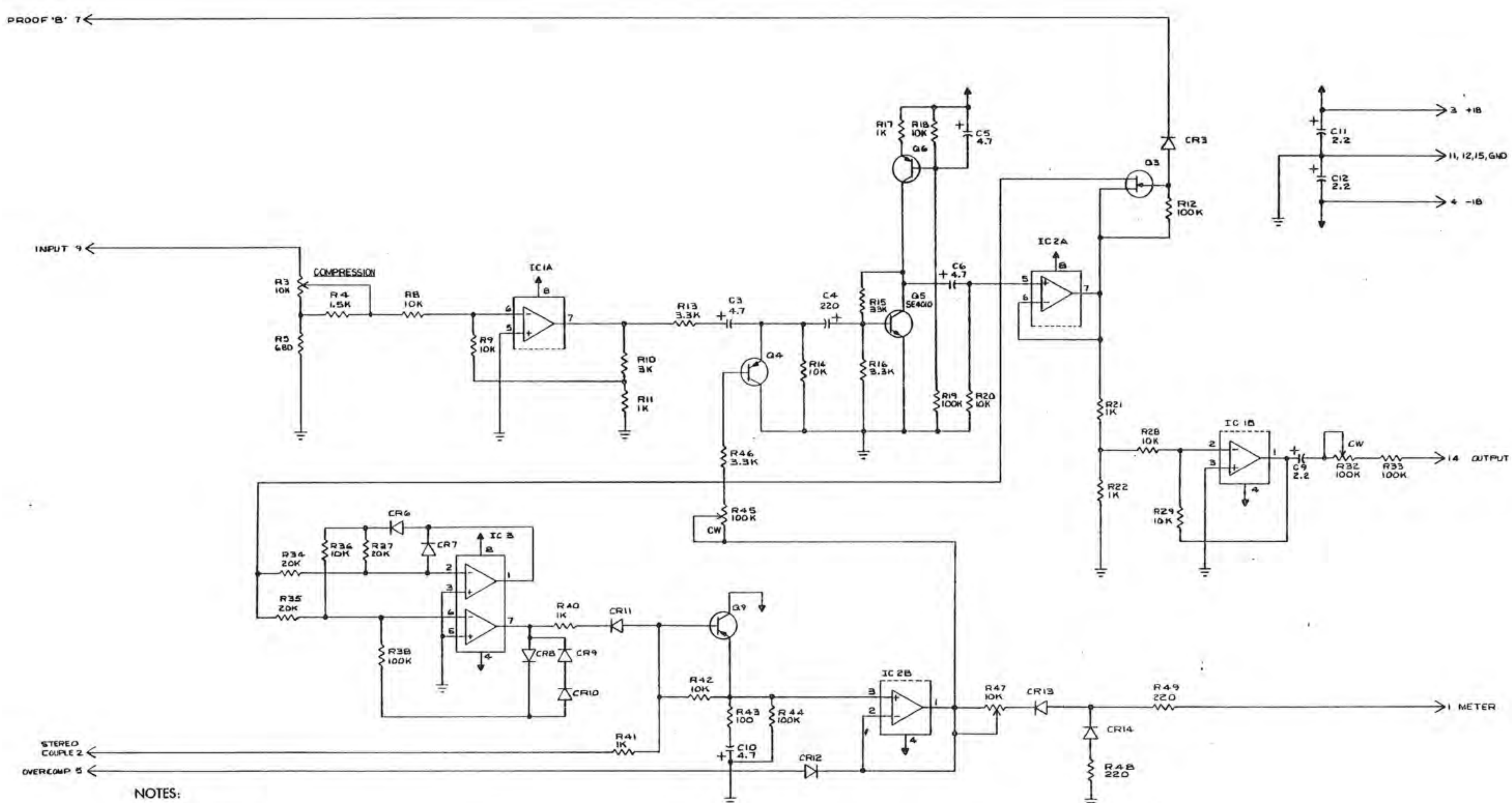
SCHEMATIC, A.G.C. AMPLIFIER

1-1 | 150000 | C

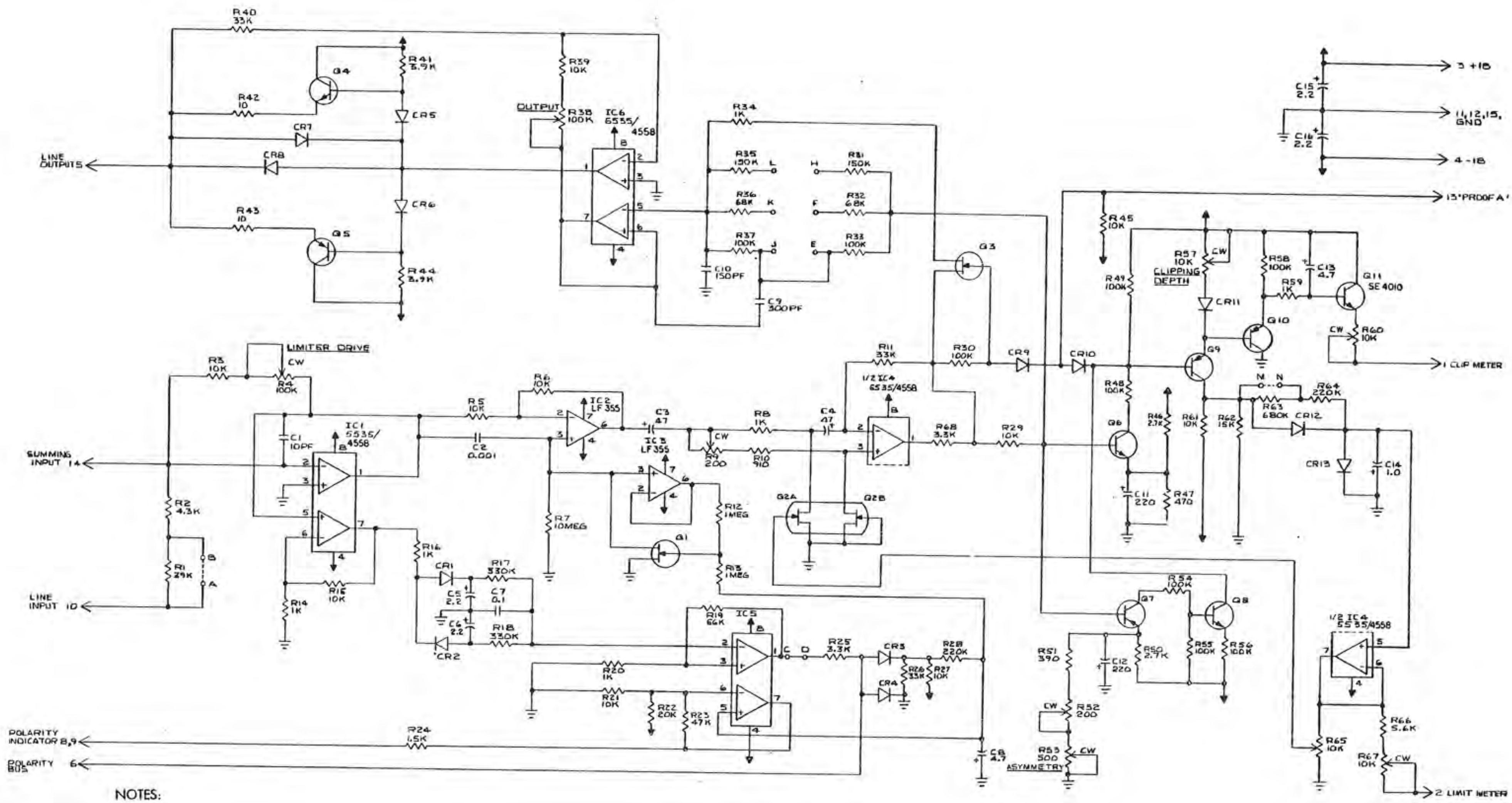


NOTES:

UNLESS OTHERWISE SPECIFIED . . . . .

1. RESISTORS ARE 1/4W, 10%; VALUE IN OHMS.
2. CAPACITORS ARE 50V, OR BETTER; VALUE IN µF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV.).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF 111 ").
6. DIODES ARE P/N 1100 (1N4003 EQUIV.).
7. IC'S ARE P/N 1313 (TYPE 4558)

215	DRAWN FAK 6-20-79 CHECKED JBW 6-20-79 APPROVED	INOVONICS INCORPORATED	
TOLERANCES	MATERIAL / FINISH —	TITLE SCHEMATIC, COMPRESSOR	
		PAGE 1 of 1	DWG NO. 152400 ISSUE A

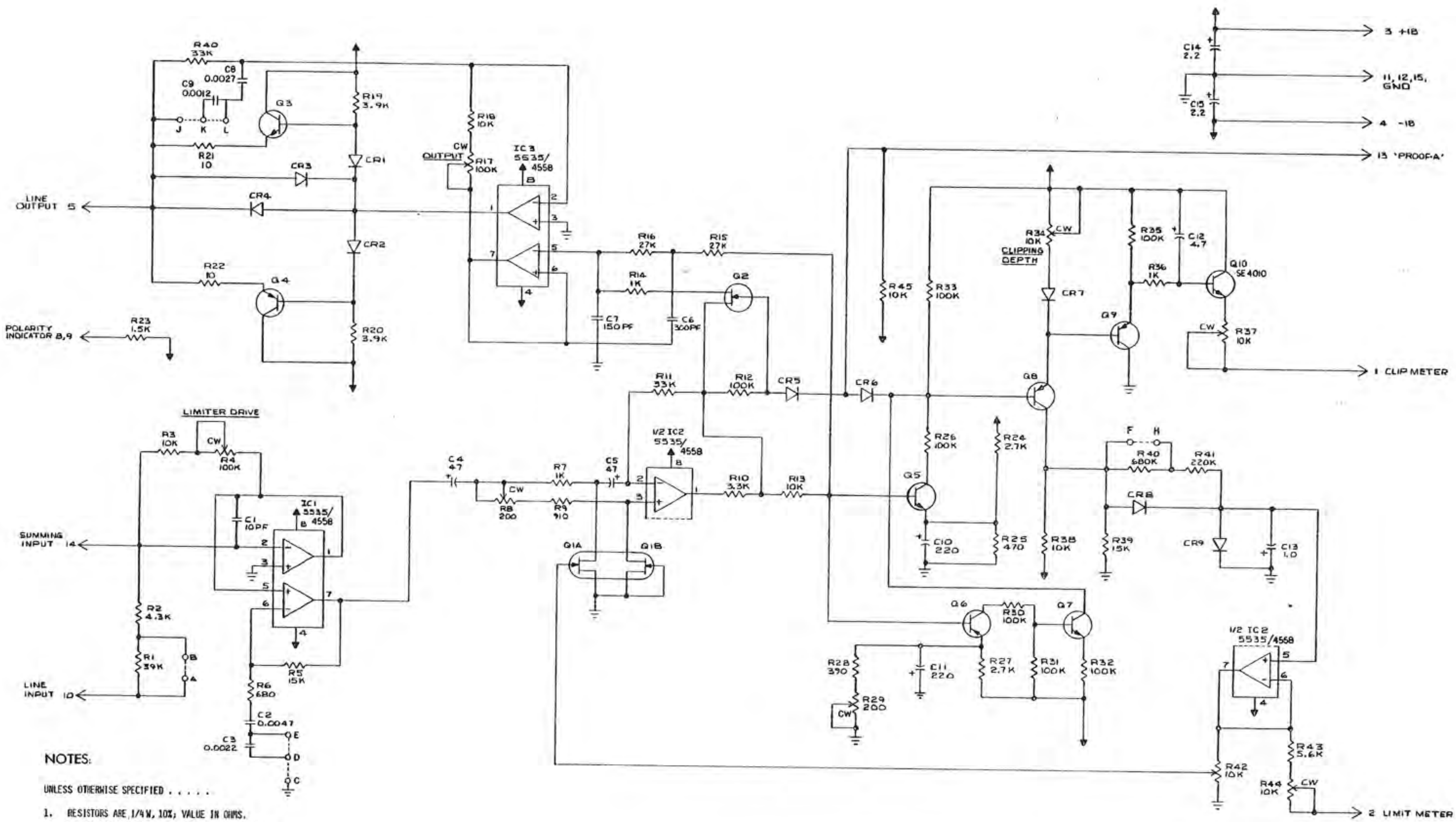


NOTES:

UNLESS OTHERWISE SPECIFIED . . . . .

1. RESISTORS ARE 1/4W, 10%; VALUE IN OHMS.
2. CAPACITORS ARE 20V, OR BETTER; VALUE IN µF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV.).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF111 ").
6. DIODES ARE P/N 1100 (1N4009 EQUIV.).

215 231	DRAWN FAK 1-25-79	INOVONICS	
	CHECKED JBW 2-8-79		
TOLERANCES	MATERIAL/FINISH	SCHEMATIC, AM PEAK CONTROLLER	
		PAGE 1 OF 1	DWG NO 150200 B

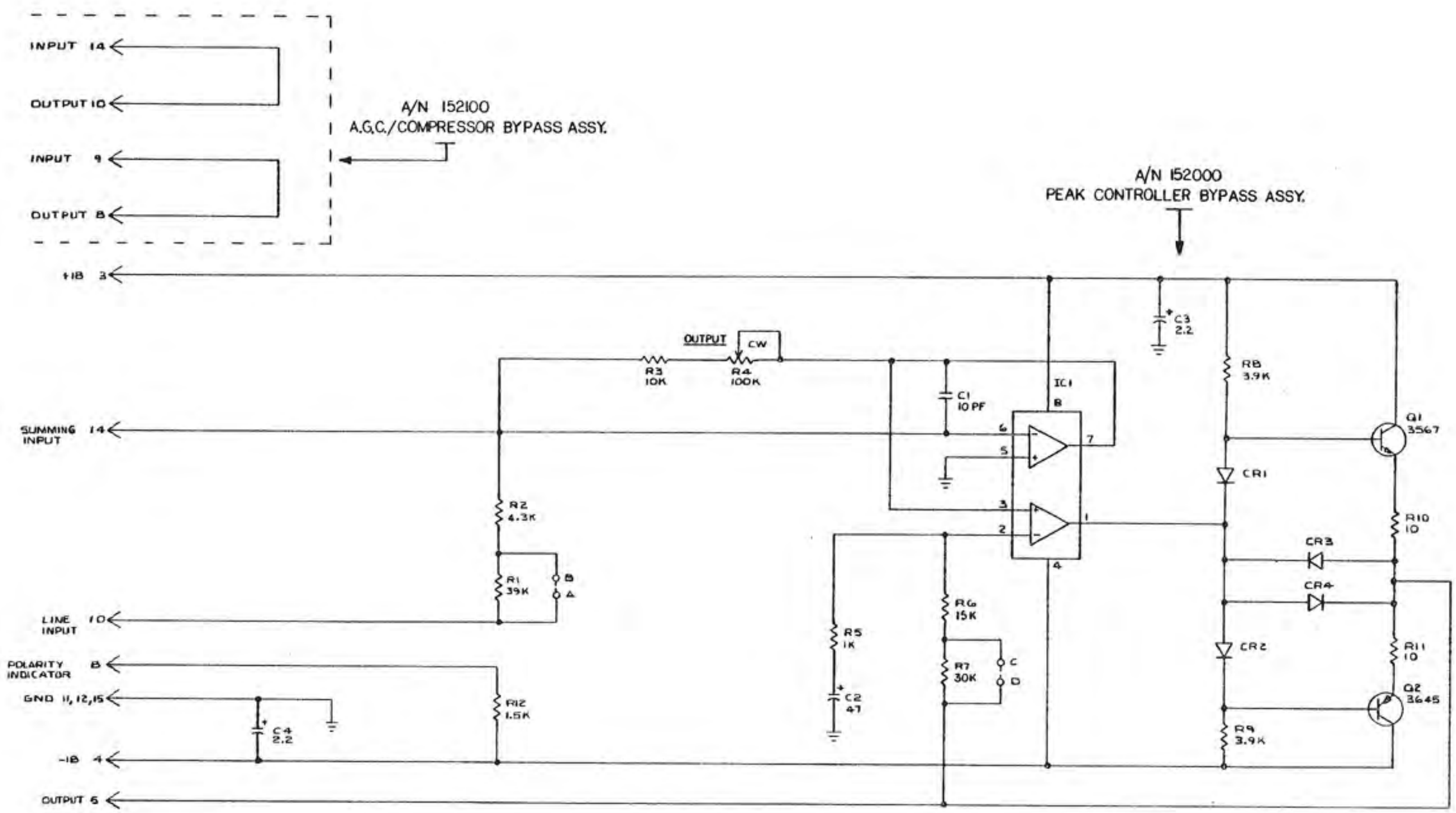


NOTES:

UNLESS OTHERWISE SPECIFIED . . . . .

1. RESISTORS ARE 1/4 W, 10%, VALUE IN OHMS.
2. CAPACITORS ARE 50 V, OR BETTER, VALUE IN µF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV.).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF 111 ").
6. DIODES ARE P/N 1100 (1N4009 EQUIV.).

215 231	DRAWN	FAK	4-3-79	INOVONICS INCORPORATED
	CHECKED	JBW	4-4-79	
	APPROVED			TITLE
TOLERANCES	MATERIAL / FINISH			F M PEAK CONTROLLER
	—			PAGE 1 of 1 · DWG NO 151000 · ISSUE A

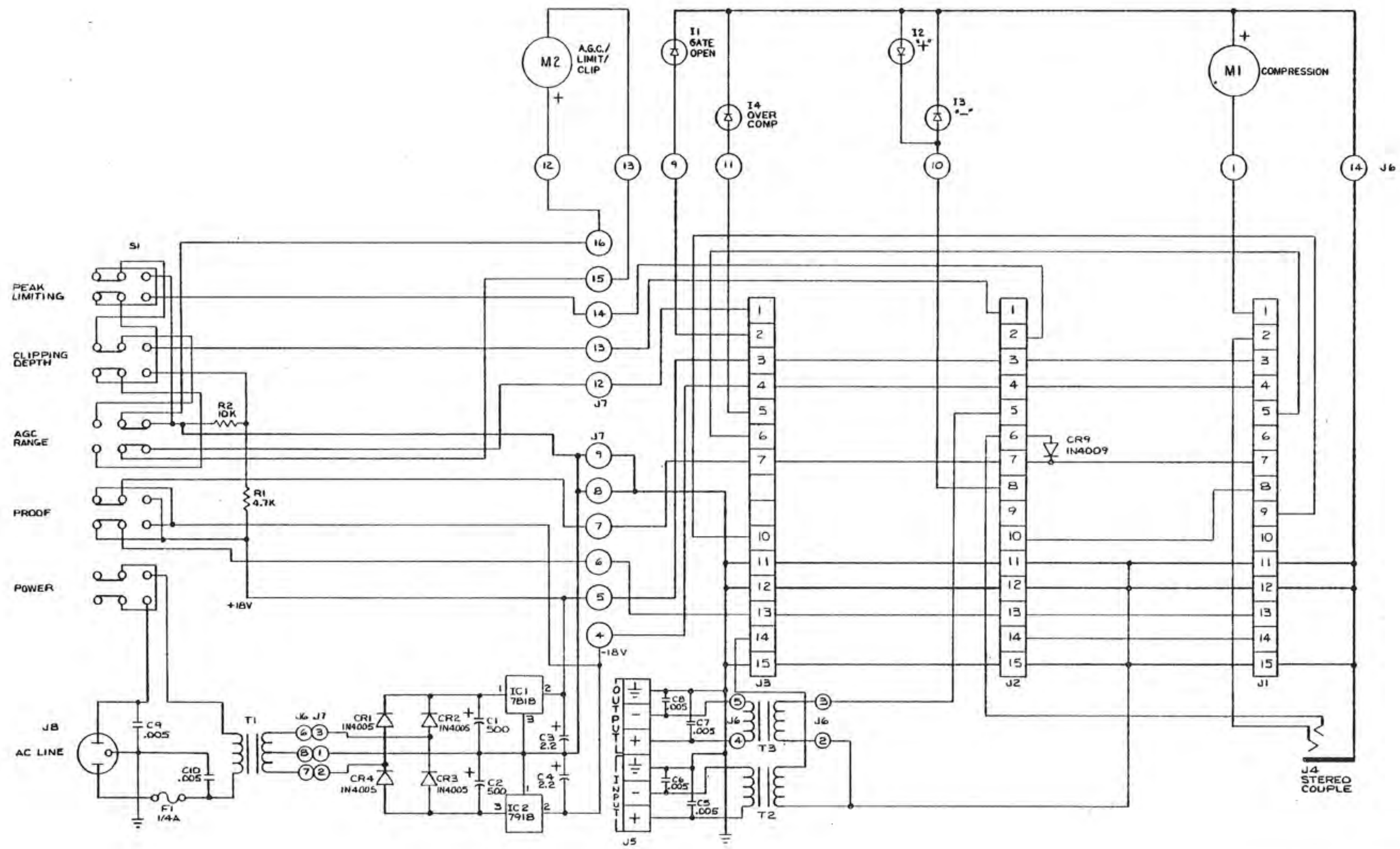


NOTES:

UNLESS OTHERWISE SPECIFIED . . . . .

1. RESISTORS ARE 1/4 W, 10%; VALUE IN OHMS.
2. CAPACITORS ARE 50 V, OR BETTER; VALUE IN µF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV.).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF 111 ").
6. DIODES ARE P/N 1100 (1N4005 EQUIV.).
7. IC'S ARE P/N 1343 (TYPE 4558)

215 231	DRAWN	FAK	5-30-79	INOVONICS INCORPORATED
	CHECKED	JBW	6-1-79	
	APPROVED			TITLE SCHEMATIC, BYPASS ASSEMBLIES
TOLERANCES	MATERIAL / FINISH —			PAGE 1 of 1 · DWG NO 152200 · ISSUE A



215	DRAWN	FAK	6-1-79	INOVONICS INCORPORATED
	CHECKED	JBW	6-5-79	
	APPROVED			TITLE
TOLERANCES	MATERIAL / FINISH	—		SCHEMATIC, CHASSIS
				PAGE 1 of 1 · DWG NO 152300 · ISSUE A

INOVONICS WARRANTY

Inovonics, Inc. products are warranted to be free from defects in material and workmanship. Any discrepancies noted within 90 days of the date of purchase will be repaired free of charge. Additionally, parts for repairs required between 90 days and one year from the date of purchase will be supplied free of charge, with installation billed at normal rates. It will be the responsibility of the purchaser to return equipment for warranty service to the dealer from whom it was originally purchased unless prior arrangement is made with the dealer to inspect or repair at the user's location.

This warranty is subject to the following conditions:

1. Warranty card supplied with the equipment must be completed and returned to the factory within 10 days of purchase.

2. Warranty is void if unauthorized attempts at repair or modification have been made, or if serial identification has been defaced, removed, or altered.

3. Warranty does not apply to damage caused by misuse, abuse, or accident.

4. Warranty valid only to original purchaser.

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